CLAIMS

1. A semiconductor device comprising:

a semiconductor substrate;

wirings formed on the substrate and separated from each other, each of the wirings including a first conductive layer pattern and an insulating mask layer pattern formed on the first conductive layer pattern;

insulating spacers formed on sidewalls of the wirings;

self-aligned contact pads including portions of a second conductive layer, each of the self-aligned contact pads in contact with surfaces of the insulating spacers to fill a gap between the wirings;

an interlayer dielectric layer formed on the contact pads, the wirings, and the substrate, the interlayer dielectric layer including contact holes that expose the contact pads; and

a selective epitaxial silicon layer formed on the contact pad exposed through the contact holes to cover the insulating mask layer pattern.

2. The semiconductor device of claim 1, wherein the insulating mask layer pattern and the insulating spacers comprise materials having an etching selectivity relative to the interlayer dielectric layer.

3. The semiconductor device of claim 2, wherein the insulating mask layer pattern and the insulating spacers comprise silicon nitride based materials.

4. The semiconductor device of claim 1, wherein the second conductive layer comprises doped polysilicon.

5. The semiconductor device of claim 1, further comprising:

contact plugs formed in the contact holes; and

contact spacers formed on the selective epitaxial silicon layer between inner sidewalls of the contact holes and the contact plugs.

6. The semiconductor device of claim 5, wherein each of the contact spacers comprises a material having an etching selectivity relative to the interlayer dielectric layer.

7. The semiconductor device of claim 6, wherein the contact spacers comprise silicon nitride based materials.

8. A method of manufacturing a semiconductor device comprising:

forming wirings separated from each other on a semiconductor substrate, each of the wirings including a first conductive layer pattern and an insulating mask layer pattern formed on the first conductive layer pattern;

forming insulating spacers on sidewalls of the wirings;

forming self-aligned contact pads including portions of a second conductive layer, each of the self-aligned contact pads making contact with surfaces of the insulating spacers to fill a gap between the wirings;

forming an interlayer dielectric layer on the substrate wherein the contact pads are formed;

partially etching the interlayer dielectric layer to form contact holes exposing the contact pads; and

forming a selective epitaxial silicon layer on the contact pads exposed through the contact holes to cover the insulating mask layer pattern.

9. The method of claim 8, wherein the insulating mask layer pattern and the insulating spacers comprise materials having etching selectivities relative to the interlayer dielectric layer.

10. The method of claim 9, wherein the insulating mask layer pattern and the insulating spacers comprise silicon nitride based materials.

11. The method of claim 8, wherein the second conductive layer comprises doped polysilicon.

12. A method of manufacturing a semiconductor device comprising:

forming wirings separated from each other on a semiconductor substrate, each of the wirings including a first conductive layer pattern and an insulating mask layer pattern formed on the first conductive layer pattern;

forming insulating spacers on sidewalls of the wirings;

forming at least two self-aligned contact pads using mask patterns having bar shapes that include openings having at least two different contact regions, each of the at least two self-aligned contact pads in contact with portions of the substrate between the wirings;

forming an interlayer dielectric layer on the substrate where the at least two self-aligned contact pads are formed;

partially etching the interlayer dielectric layer to form a contact hole exposing one of the at least two self-aligned contact pads; and

forming a selective epitaxial silicon layer on the one of the at least two self-aligned contact pads to cover the insulating mask layer pattern.

13. The method of claim 12, wherein the insulating mask layer pattern and the insulating spacers comprise materials having etching selectivities relative to the interlayer dielectric layer.

14. The method of claim 13, wherein the insulating mask layer pattern and the insulating layer spacers comprise silicon nitride based materials.

15. The method of claim 12, wherein forming at least two different contact pads comprises:

forming a first interlayer dielectric layer on the insulating spacers, the wirings, and the substrate;

etching the first interlayer dielectric layer using the insulating mask layer pattern until the portions of the substrate between the wirings are exposed;

forming a second conductive layer on the first interlayer dielectric layer and the portions of the substrate between the wirings; and

planarizing the second conductive layer and the first interlayer dielectric layer until a surface of the insulating mask layer pattern is exposed.

16. The method of claim 15, wherein planarizing the second conductive layer and the first interlayer dielectric layer is performed using a process selected from the group consisting of a CMP process, an etch-back process, and a combination of the CMP and etch-back processes.

17. The method of claim 12, wherein the contact hole is formed to have a line shape so that the one of the at least two self-aligned contact pads and another self-aligned contact pad arranged in a direction substantially parallel to the wirings are simultaneously exposed through the contact hole.

18. The method of claim 12, further comprising:

after forming the selective epitaxial silicon layer, forming contact spacers on inner sidewalls of the contact holes using the selective epitaxial silicon layer as an etching stopper; and

forming a third conductive layer in the contact hole that is electrically connected to the one of the at least two self-aligned contact pads.

19. The method of claim 18, wherein the contact spacers comprise a material having an etching selectivity relative to the interlayer dielectric layer.

20. The method of claim 19, wherein the contact spacers comprise a silicon nitride based material.

21. A method of manufacturing a semiconductor device comprising:

forming gate lines that cross active regions on a semiconductor substrate, wherein each of the gate lines includes a gate mask layer pattern and gate spacers formed on sidewalls of the gate mask layer pattern so that storage node contact regions and bit line contact regions are formed on portions of the substrate between the gate lines;

forming first contact pads connected to the storage node contact regions and second contact pads connected to the bit line contact regions using self-aligned contact mask patterns having bar shapes that include openings exposing the active regions;

forming an interlayer dielectric layer on the substrate where the first and second contact pads are formed;

partially etching the interlayer dielectric layer to form storage node contact holes having line shapes so that one first contact pad and an adjacent first contact pad arranged in a direction substantially parallel to the gate lines are exposed by each of the storage node contact holes;

forming a selective epitaxial silicon layer on the first contact pads exposed by the storage node contact holes to cover the gate mask layer patterns; and

forming storage node contact plugs in the storage node contact holes, wherein the storage node contact plugs are electrically connected to the first contact pads.

22. The method of claim 21, wherein the gate mask layer pattern and the gate spacers comprise silicon nitride based materials.

23. The method of claim 21, wherein forming first contact pads and second contact pads comprises:

forming a first interlayer dielectric layer on the gate lines and the substrate;

etching the first interlayer dielectric layer using the self-aligned contact mask patterns until the storage node contact regions and the bit line contact regions are exposed between the gate lines;

forming a first conductive layer on the first interlayer dielectric layer, the storage node contact regions, and the bit line contact regions; and

planarizing the first conductive layer and the first interlayer dielectric layer until the gate mask layer patterns are exposed.

24. The method of claim 23, wherein planarizing the first conductive layer and the first interlayer dielectric layer is performed using a process selected from the group consisting of a CMP process, an etch-back process, and a combination of the CMP and the etch-back processes.

25. The method of claim 21, further comprising, before forming the storage node contact plugs, forming contact spacers on inner sidewalls of the storage node contact holes using the selective epitaxial silicon layer as an etching stopper.

26. The method of claim 25, wherein the contact spacers comprise a silicon nitride based material.

27. The method of claim 21, wherein forming storage node contact plugs comprises:

forming a second conductive layer on the interlayer dielectric layer to fill the storage node contact holes; and

planarizing the second conductive layer until a surface of the interlayer dielectric layer is exposed, thereby separating the storage node contact plugs into node units.

28. The method of claim 21, further comprising:

before forming the interlayer dielectric layer, forming a second interlayer dielectric layer on the substrate where the first and second contact pads are formed;

partially etching the second interlayer dielectric layer to form bit line contact holes exposing the second contact pads on the bit line contact regions;

forming a first selective epitaxial silicon layer on the second contact pads exposed through the bit line contact holes to cover the gate mask layer patterns; and

forming bit lines on the second interlayer dielectric layer to fill the bit line contact holes, wherein the bit lines are electrically connected to the second contact pads through the bit line contact holes.